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EXAMINER	
LAXTON, GARY L	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,664	HIRST, MARK	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 15, 16, 20, 21, 23, 24 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Brulhart et al (US 6,259,306).

Claims 1-4; Brulhart et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain. The FETs are N type MOSFETS and power MOSFETS. The first and second diodes include turn-on voltages less than or equal to 1.2 volts.

Claims 5-7: Brulhart et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first drain and a first cathode coupled to the first source; and a second diode having a second anode coupled to the second drain and a second cathode coupled to the second source. The first and second FETs are P type MOSFETS and power MOSFETS.

Claims 15, 16, 20 and 21; Brulhart et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first gate, a first drain, and a common source; a second FET having a second gate, a second drain and the common source; a first diode having a first anode coupled to the common source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the common source and a second cathode coupled to the second drain. The first gate is coupled to the second gate. The FETs are N type MOSFETS and power MOSFETS.

Claims 23 and 24. Brulhart et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain, wherein the first and the second FETS receive an alternating current at the first and the second drain and wherein the coupled first and second source and the coupled first and second gate to facilitate switching the

alternating current through the alternating current switch. The first and second diode include turn-on voltages less than or equal to 1 .2 volts.

Claim 27; a method of switching alternating current comprising: receiving alternating current (AC) from a source; and applying the alternating current across drains of two MOSFET devices of a switch, where the two MOSFET device having a common source region, and their gates are coupled together, and the switch further having diodes that are anti-parallel to each MOSFET device, flowing the alternating current though the common source region.

4. Claims 1-4, 8, 9,13-16, 19-21 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al (US 6,236,192).

Claims 1-4; Suzuki et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain. The FETs are N type MOSFETS and power MOSFETS. The first and second diodes include turn-on voltages less than or equal to 1.2 volts.

Claims 8, 9, 13 and 14; Suzuki et al disclose an alternating current switching circuit including; a first Field Effect Transistor (FET) having a first source, a first gate and a first drain, a second FET having, a second drain, a second source coupled to the first source and a second gate coupled to the first gate, a first diode having a first anode coupled to the first source and a

first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain; and a switch control circuit coupled to the first gate and the second gate and coupled to the first source and the second source, the switch control circuit to facilitate operation of the alternating current switching circuit at frequencies greater than 200 Hz. A load is coupled to the alternating current switching circuit; the switch control circuit uses pulse width modulation. Filtering circuitry at the load. The switch control circuit is configured to operate the alternating current switching circuit at frequencies greater than 20 kHz.

Claims 15, 16 and 19-21; Suzuki et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first gate, a first drain, and a common source; a second FET having a second gate, a second drain and the common source; a first diode having a first anode coupled to the common source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the common source and a second cathode coupled to the second drain. The first gate is coupled to the second gate. The first gate is coupled to the second gate and wherein the alternating current switching circuit further comprises a switch control circuit coupled to the coupled gates and the common source, the switch control circuit to facilitate operation of the alternating current switching circuit at frequencies greater than 200 Hz. 20. The first FET and the second FET are power MOSFETS. The first FET and the second FET are N-type MOSFETS.

Claims 23 and 24; Suzuki et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a

second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain, wherein the first and the second FETS receive an alternating current at the first and the second drain and wherein the coupled first and second source and the coupled first and second gate to facilitate switching the alternating current through the alternating current switch. The first diode and the second diode include turn-on voltages less than or equal to 1 .2 volts.

Claims 25 and 26; Suzuki et al disclose a method of switching alternating current comprising: receiving alternating current (AC) from a source; switching said alternating current utilizing a MOSFET switch having two MOSFET devices with coupled sources and coupled gates and diodes anti-parallel to each MOSFET device; and controlling the switching of said alternating current, by said MOSFET switch, at frequencies greater than 200 Hz. The method of claim 25 further comprising providing switched AC to a load.

Claim 27; Suzuki et al disclose a method of switching alternating current comprising: receiving alternating current (AC) from a source; and applying said alternating current across drains of two MOSFET devices of a switch, where the two MOSFET device having a common source region, and their gates are coupled together, and the switch further having diodes that are anti-parallel to each MOSFET device, flowing said alternating current though said common source region.

Claim 28; Suzuki et al disclose a device comprising: means for switching alternating current; and means for controlling switching coupled to the means for switching alternating

current, the means for controlling switching to facilitate operation of the means for switching alternating current at frequencies greater than 200 Hz.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 17, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brulhart et al (US 6,259,306) in view of Sugawara (US 5,635,826).

Claims 17 and 18; Brulhart et al disclose the claimed subject matter in regards to claims 8 and 15 supra, except for a series resistor and capacitor circuit coupled to the first drain and the second drain; and that the series resistor and capacitor dissipate energy in the alternating current switching circuit.

Sugawara teach using snubber circuits across an alternating current switching circuit (7) to snub excess energy stored in the circuit. The snubber comprises a series connection of a resistor and capacitor.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Brulhart et al in order to utilize a series resistor and capacitor circuit coupled to the first drain and the second drain of the alternating current switching circuit to dissipate energy in the alternating current switching circuit as taught by Sugawara.

Claim 22; Brulhart et al disclose the claimed subject matter in regards to claim 15 supra, except for a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

Sugawara teach using a device (6) having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

However, the device of Sugawara uses more than four pins since Sugawara is driving two alternating current switching circuits. It is clearly obvious that if Sugawara were to drive only one alternating current switching circuit then only four pins would be required. A first pin would be coupled to the first and the second gate as shown in figure 1, a second pin coupled to the common source as shown in figure 1, a third pin coupled to the first drain (at L1 and coupled through switch 7) and a fourth pin coupled to the second drain as shown in figure 1.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Brulhart et al in order to utilize a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain in order to drive the alternating current switching circuit as taught by Sugawara.

7. Claims 10, 11, 17, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Sugawara (US 5,635,826).

Claims 10, 11, 17 and 18; Suzuki et al disclose the claimed subject matter in regards to claims 8 and 15 supra, except for a series resistor and capacitor circuit coupled to the first drain and the second drain; and that the series resistor and capacitor dissipate energy in the alternating current switching circuit.

Sugawara teach using snubber circuits across an alternating current switching circuit (7) to snub excess energy stored in the circuit. The snubber comprises a series connection of a resistor and capacitor.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize a series resistor and capacitor circuit coupled to the first drain and the second drain of the alternating current switching circuit to dissipate energy in the alternating current switching circuit as taught by Sugawara.

Claim 22; Suzuki et al disclose the claimed subject matter in regards to claim 15 supra, except for a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

Sugawara teach using a device (6) having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

However, the device of Sugawara uses more than four pins since Sugawara is driving two alternating current switching circuits. It is clearly obvious that if Sugawara were to drive only one alternating current switching circuit then only four pins would be required. A first pin would

be coupled to the first and the second gate as shown in figure 1, a second pin coupled to the common source as shown in figure 1, a third pin coupled to the first drain (at L1 and coupled through switch 7) and a fourth pin coupled to the second drain as shown in figure 1.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Brulhart et al in order to utilize a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain in order to drive the alternating current switching circuit as taught by Sugawara.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Brulhart et al (US 6,259,306).

Suzuki et al disclose the claimed subject matter in regards to claim 8 supra, except for charge pump circuitry coupled to an alternating current power source and the switch control circuit.

Brulhart et al teach using charge pump circuitry (510, 520) coupled to switch control circuitry (500a , 500b) to drive an alternating current switching circuit in order to provide the proper voltage to the gates of the alternating current switching circuit transistors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize charge pump circuitry coupled to an alternating current power source and the switch control circuit in order to provide the proper voltage to the gates of the alternating current switching circuit transistors as taught by Brulhart et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary L. Laxton
Primary Examiner
Art Unit 2838

7/22/05